6. The memory of claim 5 additionally comprising datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexors positioned at certain of said intersections of said I/O lines and said datalines for transferring signals on said I/O lines to said datalines.

7. The memory of claim 6 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

8. The memory of claim 7 wherein said plurality of peripheral devices includes a plurality of data in buffers response to data available at said plurality of pads and a plurality of data write multiplexors responsive to said plurality of data in buffers and wherein said array I/O blocks are responsive to said plurality of data write multiplexors.

9. The memory of claim 8 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

10. The memory of claim 9 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

11. The memory of claim 3 wherein said metal conductors form a web around each array block and a grid within each array block.

12. The memory of claim 3 additionally comprising switches for disconnecting each of said plurality of array blocks from said power supply.

13. The memory of claim 12 wherein said power supply has a modular design such that certain modules can be shut down in response to the number of array blocks connected to said power supply.

14. The memory of claim 1 wherein said power supply has a modular design such that certain modules can be shut down in response to a refresh mode of operation.

15. The memory of claim 1 wherein said pads are centrally located.

16. The memory of claim 15 wherein said power supply is positioned proximate to said pads.

17. The memory of claim 1 wherein said power supply includes a voltage regulator for producing an array voltage, voltage pumps for producing boosted voltages, and a voltage generator for producing a bias voltage for use by said random access memory.

18. The memory of claim 17 additionally comprising a sequence circuit for controlling the sequence in which said voltage regulator, voltage pumps, and voltage generator are powered up.

19. A memory fabricated on a die, comprising:

a plurality of memory cells providing at least 256 meg of storage;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells;

a power supply;

a plurality of pads; and

layers of metal conductors for providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads, and wherein the die is approximately 24.7 mm by 15 mm.

20. The memory of claim 1 wherein said layers of metal do not exceed two.

21. The memory of claim 19 wherein said plurality of memory cells is arranged into a plurality of individual arrays, said individual arrays being organized into rows and columns to form a plurality of array blocks.

22. The memory of claim 21 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

23. The memory of claim 23 additionally comprising digitlines extending through each of said plurality of individual arrays and into said sense amplifiers, and I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

24. The memory of claim 23 additionally comprising datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexors, positioned at certain of said intersections of said I/O lines and said datalines for transferring signals on said I/O lines to said datalines.

25. The memory of claim 24 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read

multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

26. The memory of claim 25 wherein said plurality of peripheral devices includes a plurality of data in buffers response to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

27. The memory of claim 26 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

28. The memory of claim 27 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

29. The memory of claim 21 wherein said metal conductors form a web around each array block and a grid within each array block.

30. The memory of claim 21 additionally comprising switches for disconnecting each of said plurality of array blocks from said power supply.

31. The memory of claim 30 wherein said power supply has a modular design such that certain modules can be shut down in response to the number of array blocks connected to said power supply.

32. The memory such that of claim 19 wherein said power supply has a modular design such that certain modules can be shut down in response to a refresh mode of operation.

33. The memory of claim 19 wherein said pads are centrally located.

34. The memory of claim 33 wherein said power supply is positioned proximate to said pads.

35. The memory of claim 19 wherein said power supply includes a voltage regulator for producing an array voltage, voltage pumps for producing boosted voltages, and a voltage generator for producing a bias voltage for use by said random access memory.

36. The memory of claim 35 additionally comprising a sequence circuit for controlling the sequence in which said voltage regulator, voltage pumps, and voltage generator are powered up.

37. A memory, comprising:

a plurality of memory cells providing at least 256 meg of storage, said memory calls being fabricated at a density of 791,350 bits per square mil;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells;

a power supply;

a plurality of pads; and

layers of metal conductors for providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads.

38. The memory of claim 37 wherein said layers of metal do not exceed two.

39. The memory of claim 37 wherein said memory is fabricated on a die approximately 24.7 mm by 15 mm.

40. The memory of claim 37 wherein said plurality of memory cells is arranged into a plurality of individual arrays, said individual arrays being organized into rows and columns to form a plurality of array blocks.

41. The memory of claim 40 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

42. The memory of claim 41 additionally comprising digitlines extending through each of said plurality of individual arrays and into said sense amplifiers, and I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

43. The memory of claim 42 additionally comprising datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers, positioned at certain of said intersections of said I/O lines and said data lines for transferring signals on said I/O lines to said data lines.

44. The memory of claim 43 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

45. The memory of claim 44 wherein said plurality of peripheral devices includes a plurality of data in buffers response to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

46. The memory of claim 45 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

47. The dynamic random access memory of claim 46 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

48. The memory of claim 40 wherein said metal conductors form a web around each array block and a grid within each array block.

49. The memory of claim 40 additionally comprising switches for disconnecting each of said plurality of array blocks from said power supply.

50. The memory of claim 49 wherein said power supply has a modular design such that certain modules can be shut down in response to the number of array blocks connected to said power supply.

51. The memory of claim 37 wherein said power supply has a modular design such that certain modules can be shut down in response to a refresh mode of operation.

52. The memory of claim 37 wherein said pads are centrally located.

53. The memory of claim 52 wherein said power supply is positioned proximate to said pads.

54. The memory of claim 37 wherein said power supply includes a voltage regulator for producing an array voltage, voltage pumps for producing boosted voltages, and a voltage generator for producing a bias voltage for use by said random access memory.

55. The memory of claim 54 additionally comprising a sequence circuit for controlling the sequence in which said voltage regulator, voltage pumps, and voltage generator are powered up.

56. A die carrying a 256 meg memory device, said die having not more than two layers of metal conductors.

57. A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of pads located centrally with respect to said array blocks;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies located proximate said plurality of pads for generating a plurality of supply voltages; and

a power distribution bus for delivering said plurality of supply voltages to said individual arrays and said plurality of peripheral devices.

58. A power distribution bus for a memory device constructed of memory blocks organized into an array, said bus comprised of a first plurality of conductors for carrying the voltages used by the array and forming a web surrounding each of the blocks of the array, and a second plurality of conductors extending from said web into each of the memory blocks to form a grid within each of the memory blocks.

59. A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage regulator comprised of a plurality of power amplifiers and wherein said power amplifiers are organized into a plurality of groups operable in one of separate and concurrent operating modes to achieve predetermined levels of output power; and

a power distribution bus for delivering said plurality of supply voltages to said array and said plurality of peripheral devices.

60. A voltage regulator for a dynamic random access memory, said voltage regulator comprising:

a voltage reference circuit for producing a reference voltage;

a plurality of power amplifiers for developing a supply voltage for supplying power to the dynamic random access memory, said power amplifiers being responsive to said reference voltage and having a gain greater than one; and

a control circuit for producing control signals for controlling said plurality of power amplifiers.

61. A dynamic random access memory, comprising:

an array of memory cells configured in separately controllable array blocks;

a plurality of peripheral devices responsive to external signals for writing data into said array blocks and for reading data out of said array blocks;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage regulator comprised of a plurality of power amplifiers and at least one of said power amplifiers being associated with each of said array blocks;

a plurality of power distribution switches; and

a power distribution bus for delivering said plurality of supply voltages to said array blocks through said plurality of switches and to said plurality of peripheral devices, and wherein

said plurality of peripheral devices includes logic for controlling each of said plurality of switches and for controlling the state of each of said power amplifiers.

62. A voltage regulator for a dynamic random access memory having an array divided into array blocks, said voltage regulator comprising:

a voltage reference circuit for producing a reference voltage;

multiple power amplifiers for developing a supply voltage, said power amplifiers arranged such that certain of said power amplifiers supply power to certain of the array blocks; and

control circuitry for disabling a power amplifier when the array block associated therewith is disabled.

63. A power supply for a dynamic random access memory having a plurality of array blocks and a plurality of pads located centrally of the array blocks, said power supply comprising:

a plurality of voltage supplies located proximate to the plurality of pads for producing supply voltages for the plurality of array blocks.

64. A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage pump comprised of a plurality of voltage pump circuits and

wherein said voltage pump circuits are organized into a plurality of groups operable in one of separate and concurrent operating modes to achieve predetermined levels of output power; and

a power distribution bus for delivering said plurality of supply voltages to said array and said plurality of peripheral devices.

65. A voltage pump for an integrated circuit, comprising:

a plurality of voltage pump circuits operable in response to a clock signal input thereto, said plurality of voltage pump circuits being divided into a plurality of groups for operation in response to an enable signal produced by the integrated circuit in one of separate or concurrent operating modes to achieve predetermined levels of power output;

an oscillator circuit for producing said clock signal; and

a regulator circuit for producing first signals for controlling said oscillator circuit.

66. A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices, one of said plurality of voltage supplies including a voltage generator producing an output voltage;

a voltage detection circuit responsive to said output voltage for producing an overvoltage signal and an undervoltage signal indicative of whether the output voltage is within a first predetermined range; and

a logic circuit responsive to said overvoltage and said undervoltage signals for providing an indication of the stability of the voltage generator.

67. A stability sensor for a voltage generator which utilizes pullup and pulldown currents for regulation purposes, said sensor comprising:

a current source responsive to one of the pullup and pulldown currents for producing a source current indicative of the current;

a resistor for generating a voltage in response to the source current; and

an overcurrent circuit responsive to said voltage for producing a signal indicative of an excessive amount of one of the pullup and pulldown current.

68. A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

a powerup sequence circuit for controlling the powering up of certain of the plurality of voltage supplies in response to the condition of previously powered up voltage supplies.

69. A powerup circuit for an integrated circuit having a voltage supply responsive to a voltage external to the integrated circuit and generating a feedback signal, said powerup circuit comprising:

a first circuit portion responsive to the external voltage for producing a first output signal indicative of whether the external voltage is above a predetermined value; and

a second circuit portion responsive to said first output signal and the feedback signal for producing a first enable signal to enable the voltage supply.

70. A dynamic random access memory, comprising:

an array of memory cells, each comprised of two storage elements;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

test mode logic for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latch circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first group of memory elements, and a write enable circuit responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

71. A method of testing a plurality of memory elements organized in a plurality of rows, comprising the steps of:

writing test data into a first row of memory elements;

latching the test data from the first row of memory elements in response to a first external signal;

writing the latched test data into a first group of memory elements in response to a second external signal;

reading the test data from the second group of memory elements; and

comparing the test data read from the second group of memory elements with the test data written to the first row of memory elements.

72. A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of peripheral devices for writing information into said memory cells and for reading information out of said memory cells, said plurality of peripheral devices including a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks; and

a plurality of voltage supplies for generating a plurality of supply voltages for use by said array blocks and said plurality of peripheral devices, and wherein

said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines, and wherein

said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

73. A data path for a dynamic random access memory having a plurality of data cells organized into rows and columns to form a plurality of individual arrays, the plurality of individual arrays organized into rows and columns to form a plurality of array blocks, with the array blocks organized into a plurality of quadrants, said data path comprising:

a plurality of sense amplifiers positioned between adjacent rows of individual arrays;

a plurality of digitlines extending through each individual array and into said sense amplifiers;

a plurality of I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines;

a plurality of datalines running between adjacent columns of individual arrays to form intersections with said I/O lines;

a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines;

a plurality of I/O blocks each responsive to said datalines from one of said plurality of array quadrants;

a plurality of data read multiplexers responsive to said array I/O blocks;

a plurality of data output buffers responsive to said plurality data read multiplexers;

a plurality of data pad drivers responsive to said plurality of data output buffers for making data read from the cells available at a plurality of pads;

a plurality of data in buffers responsive to data available at the plurality of pads; and

a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

74. An output buffer, comprising:

a plurality of output drive transistors connected in series between a first voltage supply and ground;

an output terminal responsive to said series connected transistors;

a latch for receiving data to be output to said output terminal;

a logic circuit responsive to said latch for controlling said output drive transistors to drive a voltage at said output terminal to one of a high and low potential representing a logic state of the data to be output;

a boot capacitor for supplying additional voltage to certain of said drive transistors;

a holding transistor responsive to said logic circuit for connecting said boot capacitor to a second supply voltage; and

a self-timed circuit path connected across said holding transistor and said boot capacitor.

75. A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into and reading data out of said array of memory cells, said peripheral devices including a plurality of programmable multiplexer cells;

a power supply;

a plurality of pads; and

layers of conductors providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads.

76. A programmable multiplexer cell for use in a memory device, comprising:

a plurality of input lines;

a plurality of output lines;

a plurality of programmable switches connecting said plurality of input lines to said plurality of output lines through said multiplexer.

77. A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays having digitlines extending therethrough, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of peripheral devices for writing data into and for reading data out of said memory cells with said digitlines;

a power supply for generating a plurality of supply voltages, said power supply voltages including a plurality of generators for producing a bias voltage for biasing said digitlines, said number of generators being equal to said number of array blocks; and

a power distribution bus for delivering said plurality of supply voltages to said plurality of array blocks and said peripheral devices.

78. A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays having digitlines extending therethrough;

a plurality of peripheral devices for writing data into and for reading data out of said memory cells with said digitlines, said peripheral devices including a plurality of sense amplifiers for sensing the signals on said digitlines, said sense amplifiers being controlled by control signals having a greater magnitude than the magnitude of the data signals to be written to said memory cells;

a power supply for generating a plurality of supply voltages; and

a power distribution bus for delivering said plurality of supply voltages to said individual arrays and said peripheral devices.

79. A sense amplifier, comprising:

a digitline for connecting an array to I/O lines;

an equalization switch adjacent the array for equilibrating said digitline;

an n-sense amplifier connected across said digitline;

a p-sense amplifier connected across said digitline;

an isolation switch connected between said n-sense and said p-sense amplifier and said equalization switch for isolating said n-sense and p-sense amplifier from the array; and

a connection switch for connecting said digitline to the I/O line.

80. A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells, said plurality of peripheral devices including a plurality of sense amplifiers;

logic for producing a redundant signal for controlling said plurality of peripheral devices,

a power supply;

a plurality of pads; and

not more than a first layer and a second layer of metal conductors providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said logic, said power supply, and said plurality of pads, said redundant signal being routed through said sense amplifiers in said second layer of metal.